Abstract of Disclosure

MULTIBIT NON-VOLATILE MEMORY AND METHOD

A memory is described having a semiconductor substrate of a first conductivity type, a first and a second junction region of a second conductivity type, whereby said first and said second junction region are part of respectively a first and a second bitline. A select gate is provided which is part of a wordline running perpendicular to said first and said second bitline.

Read, write and erase functions for each cell make use of only two polysilicon layers which simplifies manufacture and each memory cell has at least two locations for storing a charge representing at least one bit.

S:\DOCS\MMA\MMA-7132.DOC
062303